REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, Claims 53-56 stand rejected under 35 U.S.C §112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim what the applicant regards as the invention. Specifically, it is the Examiner's position that it is unclear what is meant by the following: "gate conductor guard ring prevents trapping of a stinger of polysilicon on said isolation region" as recited in Claim 53. Claims 54 and 55 are dependent on Claim 53 and allegedly are indefinite for the same reason.

In response to the §112, second paragraph rejection, applicants have amended Claim 53 to positively recite that the gate conductor guard ring prevents trapping of a stringer of *gate conductor polysilicon* on said isolation region. Support for this amendment to Claim 53 is found at Page 3, lines 9-11 of the specification of the instant application. The gate conductor polysilicon is a component of the MOSFETs located in the various regions of the claimed structure.

In view of the above amendment and remarks, the rejection under 35 U.S.C. §112, second paragraph, has been obviated; therefore reconsideration and withdrawal of the instant rejection are respectfully requested.

Claims 53-56 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over U.S. Patent No. 5,945,704 to Schrems, et. al. ("Schrems, et al.") in view of U.S. Patent No. 6,174,756 to Gambino, et al. ("Gambino, et al.") and U.S. Patent No.

6,075,720 to Leung, et al. ("Leung, et al."). Claims 57-59 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Schrems, et. al. in view U.S. Patent No. 5,897,371 to Yeh, et al. ("Yeh, et al.") and Gambino, et al.

Applicants submit that the Examiner has failed to meet his burden to provide a *prima facia* case of evidence, because the applied references fail to teach or suggest applicants' claimed structure comprising a gate conductor guard ring formed around an array region on top of an isolation region, as recited in amended Claim 53. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

First, with respect to Claim 53, the Examiner has noted on Page 3 of the instant Office Action, that the principle reference, i.e., Schrems, et al., fails to disclose the following: at least a gate conductor guard ring formed around an array region on top of said isolation region, wherein said gate conductor guard ring prevents trapping of a stringer of gate conductor polysilicon on said isolation region. Since Schrems, et al. do not teach or suggest the presence of a guard ring, and the fact that the principle reference does not teach or suggest the presence of a support region, let alone a support region that is separated from the array region by a gate conductor guard ring positioned atop an isolation region, Claims 53-56 are not rendered obvious by Schrems, et al.

Gambino, et al. fail to fulfill the deficiencies of the primary reference, Schrems, et al., since the applied secondary reference also fails to teach or suggest, "at least a gate conductor guard ring formed around an array region on top of said isolation region, wherein said gate conductor guard ring prevents trapping of a stringer of gate

conductor polysilicon on said isolation region", as recited in amended Claim 53. Gambino, et al. disclose a method for forming deep junction implants in one region of the device without affecting the implant of a second region of the intergrated circuit. Gambino, et al. disclose an array region **130**; a support region **110**; and an isolation region **150**. Gambino, et al. do not teach or suggest a gate conductor guard ring and therefore fail to teach or suggest forming a gate conductor guard ring atop an isolation region, as recited in amended Claim 53. As such, Claims 53-56 are not rendered obvious by the combined disclosures of Schrem, et al. and Gambino, et al.

Leung, et al. also fail to fulfill the deficiencies of the applied references, since this secondary reference also fails to teach or suggest, "at least a gate conductor guard ring **65** formed around an array region **12** on top of said isolation region **16**, wherein said gate conductor guard ring **65** prevents trapping of a stringer of gate conductor polysilicon on said isolation region **16**", as recited in amended Claim 53.

Applicants observe referring to Column 5, line 34-38, that Leung, et al. make a single reference to a guard ring in order to indicate that "because the n-channel transistor source-substrate is a forward biased in the Vbb circuit generator and the wordline driving circuit, special layout precautions, should be taken to provide adequate guard rings in those circuits to prevent latch-up from occurring." No further details are provided throughout the disclosure concerning the positioning of the guard ring. The sole reference to a "guard ring" is only to convey that precautions should be taken to avoid latch-up, but the reference does not teach or suggest any structural details concerning the placement of a guard ring around an array region or atop an isolation region.

It is the Examiner's position, referring to the present Office Action, that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Schrems to include a guard ring as disclosed in Lueng, et al. because it aids in preventing latch-up from occurring." Applicants respectfully disagree and submit the following.

Applicants disclose, referring to Page 3, lines 5-11 of the present specification, that the trapping of a stringer of polysilicon in the isolation region can be avoided by positioning a gate conductor guard ring **65** around the array region of a MOSFET/EDRAM structure and atop an isolation region **16**. Applicants further disclose, referring to Page 3, lines 5-11, that the presence of the gate conductor guard ring **65** provides an internal protection scheme, which prevents the designer from placing a gate conductor across the isolation region **16**; therefore reducing the incidence of stringer formation. In order for the gate conductor guard ring **65** to prevent the designer from depositing gate conductor across the isolation region **16**; the gate conductor guard ring **65** must be atop the isolation region **16**, as depicted in FIGS. 9-12.

Lueng, et al. teach away from applicants' invention since Lueng, et al. disclose the use of a guard ring in a manner that would reduce the incidence of latch-up and therefore do not position the guard ring atop the isolation region, as recited in amended Claim 53. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

Latch-up is a condition under which current flows through a silicon substrate between NMOS and PMOS regions of a CMOS structure and degrades its'

performance. Latch-up occurs under certain bias conditions, such as forward bias as disclosed in Lueng, et al., in which two transistors "latch" and provide a high conductivity path through the Si substrate between the NMOS and PMOS parts of the device. This high conductivity path between the PMOS and NMOS parts of the device eventually shorts the circuit.

Lueng, et al. disclose the desire to position guard rings to avoid latch-up. To reduce the incidence of latch-up the current that flows through the substrate to latch the NMOS and PMOS portion of the device must be reduced. Therefore in order for the guard rings disclosed in Lueng, et al., to reduce latch-up the guard rings must be within the substrate. If the guard rings where atop the isolation region, as recited in amended Claim 53, there would be no mechanism to reduce the current through the substrate between the latched portions of the device. Therefore, since Lueng, et al. disclose the use of guard rings to reduce the incidence of latch-up, the prior art reference teaches away from applicant's claimed structure where a gate conductor guard ring **65** is deposited atop an isolation region **16** in a manner that would prevent the placement of gate conductor polysilicon across an isolation region **16**. Therefore, Lueng, et al. do not teach or suggest positioning a gate conductor guard ring atop **65** atop an isolation region **16** to prevent the trapping of a stringer of gate conductor polysilicon in the isolation region **16**, as recited in amended Claim 53.

Applicants find no motivation in the combined disclosures of Schrems, et. al., Gambino, and Leung, et al. to modify their disclosed structures to arrive at applicants' claimed structure recited in Claims 53-56. There is no motivation in the applied references that teaches or suggests modifying the structures disclosed therein to include

applicants' claimed structure which includes a gate conductor guard ring **65** formed around an array region and atop an isolation region **16**, as recited in Claim 53. This rejection is thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

In light of the above remarks, applicants respectfully request that the rejection to Claims 53-56 under 35 U.S.C. §103 citing the combined disclosures of Schrems, et al., Gambino and Leung, et al. be withdrawn.

In regard to the obviousness rejection of Claims 57-59 based on the combination of Schrems, et al., Yeh, et al., and Gambino, et al.; Claim 57 recites "a dual workfunction high-performance support MOSFET/EDRAM array comprising at least one support region having a local interconnect formed therein, and at least one array region having at least one wordline formed therein, said at least one array region and said at least one support region are separated by an isolation region, and at least one wordline and said local interconnect are comprised of identical material".

Applicants submit that the applied references do not fulfill the requirements to support a prima facie case of obviousness with respect to Claim 57. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970). Schrems, et al. disclose only an array region of a device. Schrems, et al. do not teach or suggest the limitation of a support region as recited in Claim 57. Further, Schrems, et al. do not teach at least one support region

having a local interconnect formed therein, where at least one wordline and said interconnect are comprised of identical material, as recited in Claim 57.

Yeh, et al. fails to fulfill the deficiencies of the primary reference, Schrems, et al., since the secondary reference also fails to teach or suggest a support region and a local interconnect formed in the support region. Therefore, because the cited references fail to provide all of the limitations of the claimed invention the requirements for a prima facie case of obviousness, under 35 U.S.C. §103(a), have not been met.

Additionally, Yeh, et al. fail to teach or suggest where the wordline and the interconnect comprise of the same material. Applicants note, referring to Column 3, lines 39-40, that Yeh, et al. disclose a list of conductive materials that could be used in contacts, vias, interconnects, wordlines, bitlines, bus, etc. A list of possible materials that could be used for electrical contact does not teach or suggest where the wordline and interconnect are both included in the same structure and comprise of the same material. Additionally, Yeh, et al. only disclose that a conductive layer **16** is deposited atop an oxide layer **18** which is atop a substrate **12**, and do not make a specific reference to whether that conductive layer comprises both interconnect and wordlines. Therefore, Yeh, et al. fail to teach or suggest a structure including an interconnect and a wordline, where the interconnect and wordline comprise the same material, as recited in Claim 57.

Gambino, et al. also fail to fulfill the deficiencies of the applied references, since this applied secondary reference also fails to teach or suggest a local interconnect formed in the support region and where the local interconnect and wordline of the device comprise the same material, as recited in Claim 57. Gambino, et al.

disclose a structure having a second region (array region) **130** and a first region **110**, where the first region comprises a semiconducting device **115**.

Applicants, referring to Page 19, lines 20-30, disclose forming a local interconnect **94** in the support region **10** of the device by implanting the substrate through a thin oxide layer **46** to form an interconnect diffusion region **90**; removing the thin oxide layer **46**; and then depositing gate conducting material **54** directly atop the substrate, where the gate conducting material **54** is in electrical contact with the interconnect diffusion region **90**. Gambino, et al. disclose where a gate oxide **160** is deposited atop a substrate followed by the deposition of a gate layer **161**, which are then patterned forming a gate stack **115** in the first region **110**. The incorporation of the gate oxide **160** into gate stack **115**, results in a gate conductor that is not in direct contact with the substrate surface. Additionally, Gambino, et al., disclose forming source and drain regions **117, 118**; further supporting that the gate stack **115** is not an interconnect but a semiconducting device, where the devices conductivity is dependent on the thickness of the gate oxide **160**. Since Gambino, et al. fail to teach or suggest an interconnect in the support region of the device, Gambino, et al. also fail to teach or suggest a structure having a wordline and interconnect, where the wordline and interconnect comprise the same material. Therefore, Gambino, et al. do not teach or suggest a support region having an interconnect, where the interconnect and wordline comprise of the same material, as recited in Claim 57.

Applicants find no motivation in the combined disclosures of Schrems, et. al., Yeh, et al.; and Gambino, et al. to modify their disclosed structures to arrive at applicants' claimed structure recited in Claims 57-59. There is no motivation in the

applied references, which suggests modifying the structures disclosed therein to include applicants' claimed structure, which includes at least one support region **14** having a local interconnect **94**, where are least one wordline **54** and the local interconnect **94** are comprised of identical material as recited in Claim 57. This rejection is thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

Based on the above remarks the rejection of the Claims 57-59 under 35 U.S.C. §103 has been obviated. Applicants respectfully request reconsideration and withdrawl of the instant rejection.

Wherefore, reconsideration and allowance of the claims of the present application is respectfully requested.

Respectfully submitted,

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